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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/645,800 | 08/22/2003 | Jin Hyung Ryu | HI-0174 | 9284 |

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| EXAMINER | |
|---|---|
| DINH, DUC Q | |
| **ART UNIT** | **PAPER NUMBER** |
| 2629 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/645,800 | RYU ET AL. | |
| | Examiner | Art Unit | |
| | Duc Q. Dinh | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is responsive to the Applicant's Amendment filed on March 07, 2008. Claims 1-7 and 13-22 are pending in the Application; claims 1, 4 and 13 are currently amended.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art, hereafter, AAPA, pages 1-8 in view of Kumar et al. (U.S Patent No. 5,876,536)

In reference to claim 1 the AAPA discloses in Figs. 3-4 a conventional (page 8, lines 5-6) driving apparatus of a plasma display panel (PDP), comprising a multi-chip module (32) in which at least one control chip having a control circuit (ASIC 26) for controlling the PDP, and at least one memory (RAM 33) are mounted on a single package (32), wherein the multi-chip module is mounted on a printed circuit board (PCB) of a control board (13) [Paragraph 0024] (the original specification discloses control board 13 is a conventional art at paragraph [0026]). The input/output lines coupling to the control chip and the memory within a single package (32) (paragraph [0013]).

The AAPA does not disclose the multi-chip model includes a plurality of green tapes for mounting the control chip and the memory.

Kumar discloses circuit boards are made by casting glass and/or ceramic powders together with an organic powders into tapes, called green are used multilayer circuit board are well known to formed multilayer printed board. (col. 1, lines 14-26)

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for the circuit board (col. 1, lines 35-37)

In reference to claim 2, the AAPA discloses the package is a ball grid type [0022].

In reference to claim 3, the AAPA discloses the multiple chip module transmits a control signal to each driving unit via the PCB (Figs. 3-4; [0021-0022].

In reference to claim 13, the AAPA discloses a plasma display panel (PDP) driving apparatus comprising:

a control board having a circuit board (13) and a multi-chip module (32) on the circuit board, the multi-chip module including a plurality of control chips (26) and a plurality of memories (33) on a single package (32), the control chip including a control circuit (ASIC) to control a PDP (the original specification discloses control board 13 is a conventional art at paragraph [0026]).

Wherein at least one of the control chip (ASIC) and at least one memory are formed on a front of the circuit package (see Fig. 4) and an input output lines are formed through the

plurality of the circuit and the I/O lines connect the at least one control chip and the at least one memory [0024-0025].

The AAPA does not disclose the multiple chip module includes a circuit package having a plurality of circuit layers.

Kumar discloses circuit boards are made by casting glass and/or ceramic powders together with an organic powders into tapes, called green are used multilayer circuit board are well known. (col. 1, lines 14-26)

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for multi layer the circuit board (col. 1, lines 16-29 and 35-37)

In reference to claim 14, refer to the rejection as applied to claim 2.

In reference to claim 15, refer to the rejection as applied to claim 3.

In reference to claim 16 the AAPA discloses a plurality of driving units to (18 at [0018]) generate and apply driving signals corresponding to control signals received from the control board (13).

In reference to claim 17, the AAPA discloses display (22) to display an image by a plasma discharge based on the driving signals applied from each of the plurality of driving units.

In reference to claim 18, the AAPA discloses wherein the control chip comprises an ASIC type (see claim 7).

In reference to claim 19, the AAPA discloses a plurality of control chips (26) mounted on the single package.

In reference to claims 20, the AAPA discloses a plurality of memories (33) mounted on the single package

4. Claims 4-7 and 21-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art, hereafter, AAPA, pages 1-8 and Figs. 1-4.

In reference to claim 4, the AAPA discloses a driving apparatus of a plasma display panel, comprising:

a control board (13) provided with a multi-chip module (32) in which at least one control chip having a control circuit (26) for controlling the PDP, and at least one memory (33) are mounted on a single package (32) the original specification discloses control board 13 is a conventional art at paragraph [0026]).;

a plurality of driving units (18A-18B of Figs. 3-4) for generating and applying a driving signal corresponding to a control signal generated from the control board (13); and a PDP (Fig. 4) for displaying an image by a plasma discharge according to the driving signal applied from each of the plurality of driving units [0020-0025].

Wherein the multichip module is mounted on a printed circuit board (13) and input/output lines connecting the at least one control chip ([0023]) and the at least one memory is not formed directly on the PCB (13) but are formed within a single package (32) as shown in Fig. 4 and paragraph [0015] and [0020]).

In reference to claim 5, the AAPA discloses wherein the package is a ball grid type.

In reference to claim 6, the AAPA discloses the control board is provided with a printed circuit board (PCB) on which at least one package is mounted [0024].

In reference to claim 7, the AAPA discloses the control chip is an ASIC type having a control circuit (Figs, 3-4).

In reference to claim 21, the AAPA discloses a plurality of control chips (26) mounted on the single package.

In reference to claim 22, the AAPA discloses a plurality of memories (33) mounted on the single package.

***Response to Arguments***

5. Applicant's arguments filed on March 07, 2008, have been fully considered but they are not persuasive.

With respect to amended claim 1 and 13, the AAPA discloses everything except the green tapes formed the control board. However, as discussed above, Kumar discloses the green tapes using to form the control board as well known in the art; therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for the multilayer circuit board formed by green tapes (col. 1, lines 35-37). In response to applicant's argument Kumar has a different filed of invention, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977

F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the multi layer green tapes of Kumar uses to formed multilayer circuit board; therefore, it would have been obvious for one of skill in the art to use the multilayer circuit board formed by green tapes of Kumar in the multi-chip module as discussed above.

With respect to claims 4-7, the AAPA shows the multi-chip module is mounted on a printed circuit board (13) and input/output lines connecting the at least one control chip are not formed directly on the PCB (13) but are formed within the single package 32 as discloses in paragraph [0020] of the AAPA.

Therefore, the rejection is maintained

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Q. Dinh whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Duc Q Dinh/
Primary Examiner,
Art Unit 2629